REMARKS

The Office Action dated May 25, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 14 and the specification have been amended. Accordingly, claims 1-26 are pending in the present application and are respectfully submitted for reconsideration.

Allowable Subject Matter

As a preliminary matter, Applicants appreciate the allowability of claims 1-26 and have amended the claims accordingly to obviate the formal issues raised in the Office Action.

Claims 1-26 Rejected under 35 U.S.C. § 112, second paragraph

Claims 1-26 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claim 1 has been amended to correct "the voltage level" to --a voltage level--.

As for the phrase "a voltage level correction circuit correcting a voltage level of a phase-combined signal produced by combining weighted outputs of said plurality of current polarity switching circuits," Applicants submit, for instance, Figure 6 and page 17 of the present disclosure as one example of the claimed recitation.

In particular, page 17, lines 10-30 provides,

> [T]the current polarity switching circuits 31 to 34 are identical in configuration, each comprising a current source switching switch 311, a sourcing type current source (first current source) 312 connected between a high potential power

> supply line (first power supply line) Vdd and the current source switching switch 311, and a sinking type current source (second current source) 313 connected between the current source switching switch 311 and a low potential power supply line (second power supply line) Vss. The weighted outputs of the current polarity switching circuits 31 to 34 are combined, and the resulting signal is output as a combined signal from the combined node Ncs (combined signal output terminal CSO) after undergoing the voltage level correction by the voltage level correction circuit 35. In Figure 6, the circuit is shown as comprising the four current polarity switching circuits 31 to 34 to which the four-phase clocks $\phi 0$, $\phi 0X$, $\phi 1$, and $\phi 1X$ are supplied as input signals, but it will be appreciated that the timing signal generating circuit (phase combining circuit) of the present invention is not limited to the configuration shown here. (Emphasis added).

Applicants further submit that the disclosure provides a "weight signal (WS) output from the D/A converter 103b," and "the weighting signal (current) WS is supplied to the drain and gate of the diode-connected transistor 313c" for additional clarification and support of the issues raised with respect to claims 1 and 14.

With respect to claims 2 and 15 where the Examiner noted that "it is unclear how the correction circuit can be constructed from 'a negative feedback circuit'," Applicants respectfully highlight, for example, Figure 18; page 26, line 32 through page 27, line 20 which support and clarify the claimed recitation. Specifically, the disclosure provides,

> Figure 18 is a block circuit diagram showing a fifth embodiment of the timing signal generating circuit according to the present invention.
>
> In the timing signal generating circuit of the fifth embodiment, the voltage level correction circuit 35 is constructed as a negative feedback circuit and, compared with the circuits previously shown in Figures 11A to 11E, the voltage levels at the combined nodes Ncs and NcsX (the center voltage Vm of the differential combined signal output

terminals CSO and CSOX) can be adjusted to the desired voltage level with a high degree of accuracy. (Emphasis added)

That is, as shown in Figure 18, the voltage level correction circuit 35 comprises a voltage level monitoring circuit 3510 which monitors the voltage levels (differential combined terminal voltage levels) at the differential combined nodes Ncs and NcsX, and a differential amplifier (operational amplifier) 3520 which takes a reference voltage Vr as an input. The voltage level monitoring circuit 3510 comprises resistive elements 3511 and 3512 connected to the respective combined nodes Ncs and NcsX, and the voltage divided between the resistive elements 3511 and 3512 is applied to the negative input terminal of the operational amplifier 3520. The positive input terminal of the operational amplifier 3520 is supplied with the reference voltage Vr.

As for the antecedent basis of the phrase "the output voltage average value" recited in claims 5 and 18, Applicants respectfully submit that the claims provide the proper antecedent basis for said phrase. Each of claims 5 and 18 recites, among other features, "wherein said voltage level correction circuit detects an output voltage average value of said timing signals, and corrects the output voltage average value of said timing signals to or near an operation point level of said amplifier." (Emphasis added.) It is submitted that the antecedent basis appears before the second recitation of the phrase.

Regarding the clarity of the phrase "negative feedback type amplifier" as recited in claims 6 and 19, Applicants respectfully highlight Figure 30 and page 37, line 25 through page 38, line19 which discloses one example of the invention as follows:

As shown in Figure 30, in the timing signal generating circuit of the 14th embodiment, the amplifying circuit 37 is configured as a negative feedback type amplifier. More specifically, the amplifying circuit 37 comprises an amplifier 370 having, for example, the circuit configuration shown in

> Figure 28A, and a resistive element 375 for negative feedback. By employing such a negative feedback amplifier for the amplifying circuit 37, stable amplification can be easily achieved. (Emphasis added).
>
> Here, if the input voltage (the voltage at the combined node Ncs) to the amplifying circuit 37 is adjusted almost to the operation point level of the amplifying circuit 37 (amplifier 370) by means of the voltage level correction circuit 35, since the feedback action of the amplifier also works to correct the operation point level, a situation where no output is produced can be avoided even when the amplifier gain per stage is raised.
>
> If a non-feedback amplifier is used, the amplitude of the voltage at the combined node Ncs (the combined signal output terminal CSO) may become too large and may exceed the saturation region of the current source transistors; if this happens, generation of the highly accurate intermediate voltage will be adversely affected. By contrast, when the amplifying circuit 37 is configured as a feedback type amplifier, as in the timing signal generating circuit of the 14th embodiment, since the input voltage to the amplifier 370 is reduced to 1/(amplifier gain) of the output voltage, a situation where a great burden is placed on the current source transistors does not easily occur.

Given the above, Applicants respectfully submit that the present application is in compliance with U.S. patent practice, and request that the rejection be withdrawn.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1-26 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-26 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 100021-00137.

Respectfully submitted,

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